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EXAMINER	
LEE, CHUN KUAN	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 05/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding..

Office Action Summary	Application No.	Applicant(s)	
	10/724,534	KLEIN, DEAN A.	
	Examiner	Art Unit	
	Chun-Kuan (Mike) Lee	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22,31-47 and 49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22,31-47 and 49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Supervisory FRITZ FLEMING PRIMARY EXAMINER 5/1/2006 GROUP 2100 AU2181

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/16/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see page 10, lines 1-8, filed on 02/16/2006, with respect to the rejection(s) of claim(s) 1-49 under 35 U.S.C. § 102(e) and 35 U.S.C. § 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Hsu et al. (US Patent 5,948,100). Claims 23-30 and 48 are canceled and claims 1-22, 31-47 and 49 are currently pending for examination.

Claim Objections

2. Claim 40 is objected to because of the following informalities:

in claim 40, line 6, "said cache memory means" should be replaced with -said cache data memory means-. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 21 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 21, it appears unclear because applicant reiterated the condition of the event resulted from the plurality of matches in the cache line, but there appears no specific claimed limitation of the result wherein there is not a plurality of matches in the cache line, therefore if is uncertain what occurs if there is not a plurality of matches in the cache line. Examiner assumes that nothing specific occurs if there is not a plurality of matches in the cache line for the current examination.

Claim Rejections - 35 USC § 102

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-4, 8, 11-16, 18, 20-21, 31-32, 36-37, 39-41, 43, 45-46 and 49 are rejected under 35 U.S.C. 102(e) as being anticipated by Hsu et al. (US Patent 5,948,100).

5. As per claims 1 and 12, Hsu teaches a method of performing a cache search operation within a digital processing system, searching a string of data for a match with a test data string, the method comprising:

receiving an instruction (interrupt comprising the STA (program start address)) to perform a search operation, the instruction comprising a test data string and a starting address for the search operation (Fig. 8-9, 14; col. 22, l. 31 to col. 23, l. 48 and col. 25,

l. 61 to col. 26, l. 8), wherein the received interrupt inherently incur the search utilizing the search address (SA) = STA, wherein SA comprises the TAG test data and the SET starting address (Fig. 9) and the search operation is perform by the branch target buffer (BTB 200 of Fig. 8 and col. 13, ll. 10-17);

routing the instruction (interrupt and STA) to a data string manipulation circuit (fetcher 400 of Fig. 8 and Fig. 14) capable of performing string manipulation instructions (col. 12, ll. 20-57), wherein the fetcher is able to manipulate by modifying (altering) the fetch address (FA) and the SA;

routing the starting address (SA comprising the SET starting address) for the search operation from the data string manipulation circuit to a cache memory array (BTB 200 of Fig. 9);

searching a cache line (cache block comprising 212, 214, 216, 218 of Fig. 9) in the cache memory for data that matches the test data string (TAG) by comparing (utilizing comparators 244-1 to 244-4 and 226-1 to 226-4 of Fig. 9) the test data string (TAG) with data stored in the cache memory array (Fig. 8-9, ref. 200), wherein said cache line comprises more bytes than the test data string (col. 13, l. 41 to col. 14, l. 65), wherein the cache block (cache line) comprises four blocks of data and the comparators attempts to match one of the four blocks to the test data string; and

routing an address (predicted target address (TA) and predicted instruction address (PA)) of cached data matching the test data string (TAG) to the data string manipulation circuit (fetcher 400 of Fig. 8) (Fig. 8).

6. As per claim 2, Hsu teaches the method additionally comprising routing the test data string (SA comprising TAG) from the data string manipulation circuit (Fig. 8, ref. 400) to the cache memory array (Fig. 8-9, ref 200).

7. As per claims 3 and 13, Hsu teaches the method additionally comprising aligning the test data string with the data stored, by utilizing an offset (OFFSET) of the start address, in the cache memory array prior to said act of comparing (Fig. 9 and col. 13, l. 42 to col. 14, l. 65), wherein the TAG is aligned utilizing OFFSET.

8. As per claims 4 and 16, Hsu teaches the method comprising wherein said act of routing an address of cached data is performed by a decoder (priority decoders 232, 234 of Fig. 9) (col. 14, l. 57 to col. 15, l. 57).

9. As per claims 8 and 18, Hsu teaches the method comprising wherein said act of comparing is performed by a plurality of comparators (Fig. 9, ref. 244-1 to 244-4 and 226-1 to 226-4) (col. 14, ll. 23-65).

10. As per claims 11 and 20, Hsu teaches the method comprising wherein said act of comparing is performed in one single clock cycle (col. 2, ll. 1-21), as each stage of a pipeline requires one cycle to perform, such as fetching one instruction per cycle.

11. As per claim 14, Hsu teaches the method comprising wherein the data string manipulation circuit comprises a bus interface unit (control logic 435 of Fig. 14), wherein the control logic interfaces between the received interrupt comprising STA and what is actually sent to the BTB.

12. As per claim 15, Hsu teaches the method comprising wherein the data string manipulation circuit comprises a memory controller (control logic 435 of Fig. 14), wherein the control logic controls the MUX (Fig. 14, ref. 425, 420), therefore controlling what is inputted and stored into the memory comprising the SA register (Fig. 14, ref. 410) and the FA register (Fig. 14, ref. 405).

13. As per claim 21, Hsu teaches the method comprising wherein said act of routing an address of the matching cached data comprises routing the address (PA and TA) of the matching cached data (Fig. 8), wherein there is not a plurality of matches in the cache block (col. 13, l. 42 to col. 14, l. 65). As applicant did not specify a condition wherein if there is not a plurality of matches in the cache line, examiner assumes there is no specific claimed limitation in regarding to said condition when occurs.

14. As per claim 31, Hsu teaches a processor comprising:

a data memory (Fig. 9, ref. 210) comprising a plurality of cache lines (Fig. 9, ref. 212, 214, 216, 218, wherein the plurality of cache blocks (cache line) comprises of four

blocks of data), each cache line comprising a plurality of bytes of data (col. 13, ll. 41-65);

an instruction processing circuit (BTB 200 of Fig. 8-9) configured to receive a test data string (TAG) and an instruction to perform a search operation beginning at a starting address (SET) of the data memory, the instruction processing circuit comprising a plurality of inputs coupled to the data memory such that each input is coupled to receive one of the plurality of bytes of data of the cache line (col. 13, ll. 41-65 and col. 16, ll. 55-61), the instruction processing circuit further comprising a plurality of outputs (outputs comprising PA and TA of Fig. 8-9), wherein upon receiving the search address (SA) the BTB inherently perform the search operation searching the plurality of cache blocks for data matching to the test data string (col. 13, ll. 11-16 and col. 13, l. 42 to col. 14, l. 65); and

a decoder (priority decoders 232, 234 of Fig. 9) coupled to the plurality of outputs of the instruction processing circuit and configured to identify a portion of the cache line having data that matches at least a portion of the test data string (TAG) (col. 14, l. 66 to col. 16, l. 10).

15. As per claim 32, Hsu teaches the processor comprising wherein the instruction processing circuit further comprises a plurality of comparators (Fig. 9, ref. 244-1 to 244-4 and 226-1 to 226-4), each comparator configured to compare at least one of the plurality of bytes of data with at least a portion of the test data string (col. 13, l. 42 to col. 14, l. 65).

16. As per claim 36, Hsu teaches the processor comprising wherein the test data string comprises a plurality of bytes (col. 13, ll. 41-65).

17. As per claim 37, Hsu teaches the processor comprising wherein the entire cache line is compared to the test data string in one bus cycle (Fig. 9 and col. 2, ll. 1-21), wherein the entire catch block (cache line) is compared in parallel and one instruction is fetched per cycle.

18. As per claim 39, Hsu teaches the processor comprising wherein the instruction processing circuit (Fig. 9, ref 200) further comprises a memory controller (output selection circuit 270 of Fig. 9) (col. 15, l. 59 to col. 16, l. 10), wherein the output selection circuit controls what is outputted from the BEB data RAM.

19. As per claim 40, Hsu teaches a cache memory circuit comprising:

a data source (SA register 410 of Fig. 14) means for holding a data value (holding the search address (SA));

a cache data memory means for holding at least one cache line comprising a plurality of bytes of data (Fig. 9, ref. 210, 212, 214, 216, 218 and col. 13, ll. 42-65), wherein the cache block (cache line) comprises of four blocks of data; and

means for searching the at least one cache line, wherein said means for searching is coupled to said cache data memory means and said data source means,

and wherein said means for searching receives a starting address (SET) for a search operating of the at least one cache line (cache block) and aligns the data value with an offset (OFFSET) of the starting address to search the at least one cache line in one clock cycle for data that matches the data value (Fig. 8-9; col. 2, ll. 1-21 and col. 13, l. 42 to col. 14, l. 65), wherein each stage of a pipeline performs in one cycle, such as fetching one instruction per cycle.

20. As per claim 41, Hsu teaches the cache memory circuit further comprising a means for decoding (priority decoders 232, 234 of Fog. 9) coupled to the means for searching (comparators 244-1 to 244-4 and 226-1 to 226-4 of Fig. 9), wherein the means for decoding identifies a portion of the cache line that matches at least a portion of the data value.

21. As per claim 43, Hsu teaches the cache memory circuit comprising wherein the means for searching comprises a plurality of comparators (Fig. 9, ref. 244-1 to 244-4 and 226-1 to 226-4).

22. As per claim 45, Hsu teaches the cache memory circuit comprising wherein the data source means comprises an external string execution circuit (fetcher 400 of Fig. 8), wherein the fetcher is external to the BTB.

23. As per claim 46, Hsu teaches the cache memory circuit comprising wherein the external string execution circuit comprises a bus interface unit (control logic 435 of Fig. 14).

24. As per claim 49, Hsu teaches the cache memory circuit comprising wherein the data value comprises a plurality of bytes (col. 13, ll. 41-65).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

25. Claims 5-7 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al. (US Patent 5,948,100) in view of Sachs et al. (US Patent 4,860,192).

Hsu teaches all the limitations of claims 1 and 12 as discussed above.

Hsu does not expressly teach the method comprising:

wherein the test data string comprises a word;

wherein the test data string comprises a doubleword; and

wherein the test data string comprises a quadword.

Sachs teaches a cache system and method

wherein the cache memory stores a singleword per addressable line of cache storage (column 7, lines 1-5);

wherein the cache memory stores a doubleword per addressable line of cache storage (column 7, lines 1-5); and

wherein the cache memory stores a quadword per addressable line of cache storage (column 2, lines 26-34).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Sachs's singleword, doubleword and quadword into Hsu's test data string.

Therefore, it would have been obvious to combine Sachs with Hsu for the benefit of enabling searching of words of multiple length, as Hsu's cache block comprises the maximum length of 16 bytes, enabling the storing up to a quadword.

26. Claims 9, 19, 33-34 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al. (US Patent 5,948,100).

Hsu teaches all the limitations of claims 8, 18, 32 and 43 as discussed above. Hsu further teaches the method comprising the plurality of bytes stored in the plurality of data blocks of the cache blocks (col. 13, ll. 41-65), to be compared for matching to the test data string by the plurality of comparators (Fig. 9, ref. 244-1 to 244-4 and 226-1 to 226-4), in parallel in one cycle (Fig. 9 and col. 2, ll. 1-21).

Hsu does not expressly teach the method comprising wherein the number of the plurality of comparators is equal to the number of bytes in a cache line of the cache

memory array; and wherein the decoder is configured to identify the matching portions of the cache line when matches from at least two comparators are detected.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made for the number of Hsu's plurality of comparators to be equal to the number of bytes in the cache block (cache line) of the cache memory array; and as the test data string comprises the plurality of bytes and the matching of the test data string requires the matching by the number of plurality of comparators equaling to the number of bytes of the test data string, therefore the matching would comprises of at least two comparators to be detected and identified by the decoder.

Therefore, it would have been obvious to implement the number of the plurality of comparators equaling to the number of bytes in the cache block for the benefit of expediting the searching as the fetching process fetches an instruction per cycle, therefore requiring the comparing of all the plurality of bytes in the cache block simultaneous in parallel in order to accomplish the fetching process.

27. Claims 10, 17, 35 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al. (US Patent 5,948,100) in view of Tran et al. (US Patent 5,764,946).

Hsu teaches all the limitations of claims 1, 31 and 40 as discussed above.

Hsu does not teach the method wherein said act of comparing is performed with a plurality of subtractors.

Tran teaches a system and a method for predicting an instruction fetch within an Instruction cache comprising:

wherein said act of fetching address is performed with a plurality of subtractors (col. 37, ll. 7-20 and col. 38, ll. 24-33).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Tran's subtractor into Hsu's act for comparing.

Therefore, it would have been obvious to combine Tran with Tran for the benefit of proper calculation of the address (Tran, col. 38, ll. 24-33).

28. Claim 38 and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al. (US Patent 5,948,100) in view of Hicks et al. (US Patent 6,085,291).

Hsu teaches all the limitation of claims 31 and 45 as discussed above.

Hsu does not expressly teach the processor wherein the data memory comprises a Level 1 cache; and wherein the external string execution circuit is associated with an off-chip memory controller.

Hicks teaches a computer system comprising:

a processor (Fig. 1, ref. 106, 108, 110) comprising of an associated L1 cache (Fig. 1 ref. 112, 114, 116); and

a memory controller (Fig. 1, ref 104), wherein the memory controller is an off-chip memory controller, external to the processor.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Hicks's L1 cache and memory controller into Hsu's processor's cache block.

Therefore, it would have been obvious to combine Hicks with Hsu because it is well known to one skilled in the art that cache memory of the processor comprises L1 cache, because the processing speed of the L1 cache is comparable to the speed of the processor, therefore enable for the processor to obtain data stored in the L1 cache much faster, in comparison to a cache memory located exterior to the processor; and further more, it is well known to one skilled in the art for the memory controller to be associated with the processor, wherein the memory controller is utilized to control the system memory of the computer system.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz M. Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

C.K.L.
04/27/2006

Supervisory FRITZ FLEMING PRIMARY EXAMINER GROUP 2100 AU2181 5/1/2006